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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,073	09/17/2003	Edward J. Crawford	FIS920000188US2	5068

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EXAMINER

TRAN, BINH X

ART UNIT PAPER NUMBER

1765

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/664,073

Applicant(s)

CRAWFORD, EDWARD J.

Examiner

Binh X. Tran

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9-17-2003</u> . | 6) <input type="checkbox"/> Other: _____ |

5.0.0

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species A (claims 1-8, 10-16 *; See Note below for further detail) in the reply filed on 7-7-2005 is acknowledged.
2. Claim 9 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 7-7-2005.

*Note: In the response filed 7-7-2005, the applicants indicates that species A includes claims 1-8, 10-33. This is incorrect because in the preliminary amendment filed 9-17-2003, applicants cancel claims 17-33. Thus, the examiner only considers that claims 1-8, 10-16 drawn to Species A.

Priority

3. The applicants claim that this application (10/664,073) is a division of Application No. 09/759,101, filed 01-12-2001, now US Patent 6,653,240. This divisional claim is improper because the current application claims and the 09/759,101 are not distinct or independent invention with each other. The MPEP 201.06 define a divisional application as "A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or 'division.'" Further, A divisional application is often filed as a result of a restriction requirement made by the examiner in the parent application. It is noticed that there is no election / restriction requirement in the parent application 09/759,101.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-8, 9-16 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2, 4-116 of U.S. Patent No. 6,653,240. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claim in the US Patents 6,653,240 is narrower by further specifying a second conductor layer.

The following table will match the claims between current invention claims and US 6,653,240

Current invention (10/664, 073) claimsUS 6,653,240 claims

1	1
2	5
3	7
4	9
5	10
6	11
7	12

Art Unit: 1765

8	2
10	8
11	5
12	13
13	14
14	15
15	16
16	4

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 3-6, 10, 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US 6,165,695) in view of Ito et al. (US 6,200,888).

Respect to claims 1 and 14, Yang teaches a method for circuit modification of micro-chip comprising at least one conductor (62) in an one organic dielectric layer (i.e. SOG or polyimide layer 66), the method comprising:

applying a protective inorganic layer (silicon 70) on the organic dielectric (66) (Fig 6, col. 7 lines 5-15);

forming a window (opening 102) in the protective inorganic surface to selectively expose an underlying portion of the organic dielectric (66), the window (opening 102) located over an area that cover the conductors (62) (Fig 11, col. 9 lines 1-8);

etching the organic dielectric through the one window (opening 102) to selectively remove a portion of the organic dielectric layer (66) adjacent to the conductor (62) (col. 9 lines 41-67, Fig 12).

Yang fails to disclose the step of performing an ion-milling process on the conductor. In a method for circuit modification, Ito discloses the step of performing an ion-milling process on the conductor layer (12) in the presence of the dielectric organic layer (polyimide layer 13) (See col. 4 lines 43-52; col. 6 lines 23-57; Fig 1B). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Yang in view of Ito by performing an ion milling process because it will help to remove the naturally oxidized film on the conductive layer.

Respect to claims 3 and 15, Yang teaches etching the organic dielectric (66) comprise reactive ion etching (RIE) (col. 9 lines 42-46). Respect to claim 4-5, Yang fails to disclose the conductive layer (62) comprise metal such as copper. In a semiconductor method, Ito teaches that the conductive layer (12) can be metal such as copper (col. 4 lines 25-27). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Yang in view of Lin by using metal comprises copper because equivalent and substitution of one for the other would produce an expected result.

Respect to claim 6, Yang teaches the protective inorganic surface layer (70) etches selectively to the organic dielectric (66) (See Fig 11). Respect to claim 10, Yang teaches the reactive ion etching is performed using CO and O₂ (col. 9 lines 55-57).

Respect to claim 12, Yang discloses a method for circuit modification comprising:

Art Unit: 1765

depositing a protective inorganic layer (70) onto an organic dielectric layer (66) into which is embedded a conductor (62) (Note: The examiner interprets that the conductor (62) is embedded in organic layer (66) since the applicants show in Fig 1A-1D of the present application that the "embedded" feature can be shown by having two layers adjacent to each other);

forming a window (opening 102) in the protective inorganic layer (70) to selectively expose an underlying portion of the organic dielectric (66) (Fig 11-12);

etching the organic dielectric through the one window (opening 102) to selectively remove a portion of the organic dielectric layer (66) adjacent to the conductor (62) (col. 9 lines 41-67, Fig 12).

The limitation regarding the conductor is to be modified ion-milling process has been discussed above. Respect to claim 13, Yang teaches etching comprise reactive ion etching (RIE) (col. 9 lines 42-46).

Respect to claim 16, Yang discloses that the conductor (62) to be modified and the organic dielectric layer (66) to be selectively removed are buried below at least one upper layer (i.e. buried below the protective inorganic layer 70 and the photoresist layer) and the method comprises successively providing an opening in each of said least one upper layer (See Fig 9-11).

9. Claims 2, 8, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Ito in view of Talbot et al. (US 6,225,626).

Ito fails to disclose the step of milling the conductor with a focused ion beam (FIB) in the presence of passivating gas xenon difluoride or the window is formed by a

Art Unit: 1765

FIB. However, Ito clearly discloses the step ion milling process. In a semiconductor method, Talbot teaches milling the conductor FIB in the presence of xenon difluoride (col. 6 lines 50-65) to form a deep window. It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Yang in view of Talbot by using the FIB in the presence of xenon difluoride because it will create a deeper window portion through the active region.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Ito and further in view of Hasegawa et al. (US 6,383,907).

Respect to claim 7, Yang fails to disclose that the inorganic protective comprises nitride. However, Yang clearly discloses that the inorganic protective layer (70) is amorphous silicon (col. 7 lines 6-10). In a semiconductor method, Hasegawa teaches that either amorphous silicon film or silicon nitride or silicon oxide nitride can be use (col. 7 lines 31-35, read on "comprise nitride"). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Yang and Ito in view of Hasegawa by using a inorganic protective layer comprise nitride because equivalent and substitution of one for the other would produce an expected result.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X. Tran whose telephone number is (571) 272-1469. The examiner can normally be reached on Monday-Thursday and every other Friday.

Art Unit: 1765

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tran

Binh X. Tran